Chemical Mechanical Planarization of TEOS SiO_2 for Shallow Trench Isolation Processes on an IPEC/Westech 372 Wafer Polisher

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- EMCR 801: MicroE Graduate Seminar
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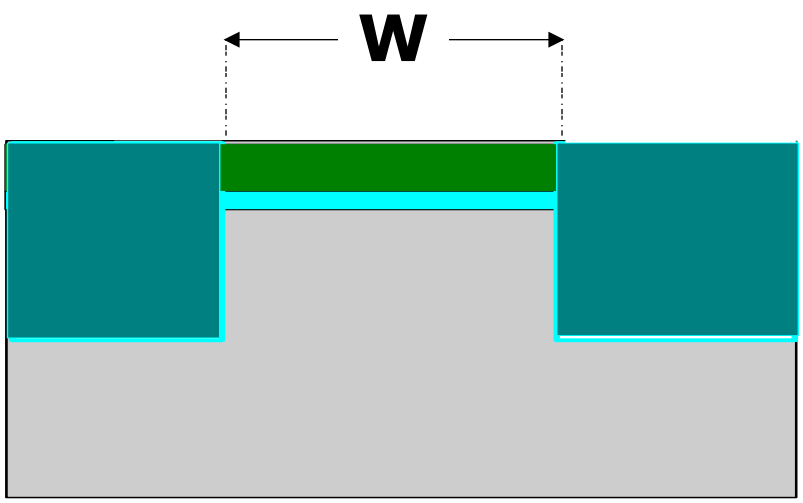
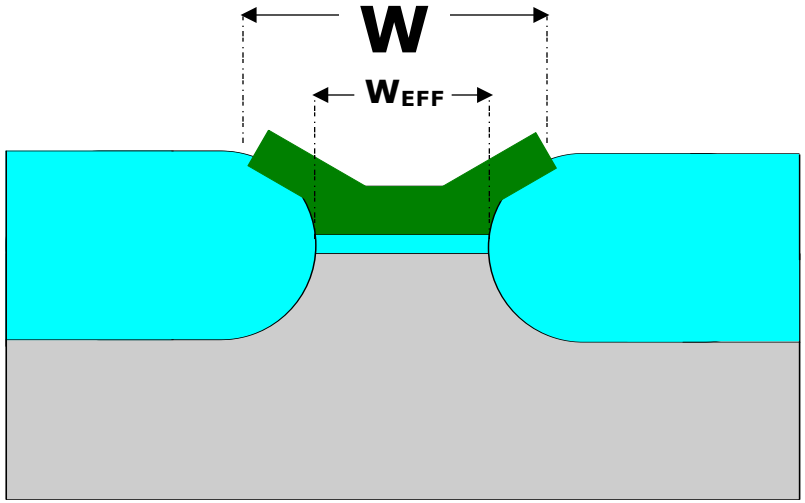
Outline

- STI vs. LOCOS
- Example STI Process
- CMP Equipment and Materials
- Westech 372 “How-To”
- CMP Results
- Process and Layout Challenges
- Questions

STI vs. LOCOS Isolation Schemes





STI

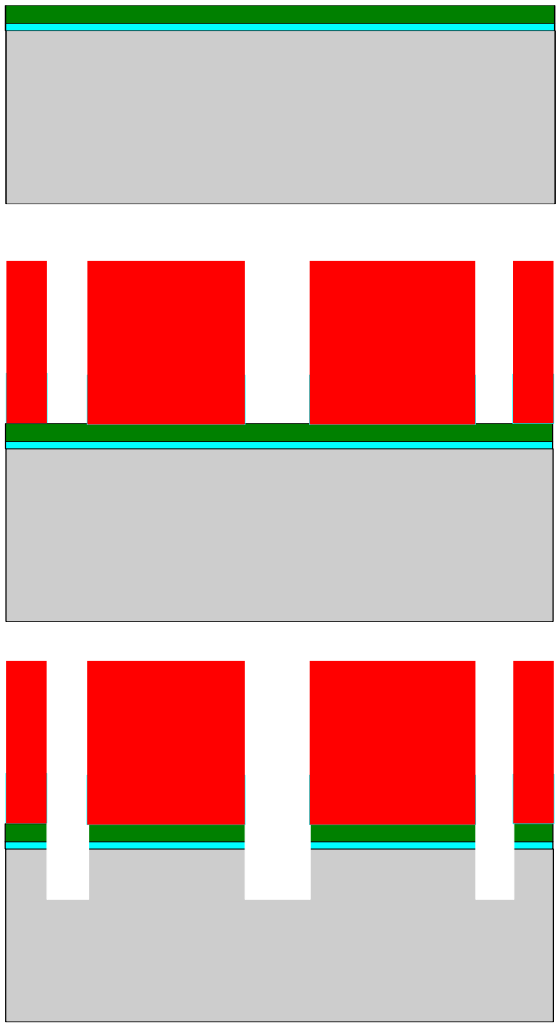
- $W_{DRAWN} \approx W_{ACTUAL}$
- Increased packing density
- Larger drive current for devices with same W_{DRAWN}
- Decreased Topography

LOCOS

- $W_{EFF} < W_{DRAWN}$ due to "Bird's Beak" Effect
- Transistors must be made wider to achieve nominal drive current, decreased packing density
- Difficult to use LOCOS < 0.5 μm

- STI is replacement of LOCOS as preferred isolation technology

Example STI Process

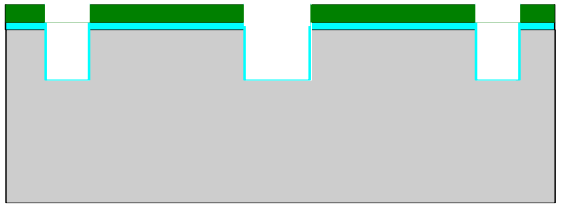


- Grow 500A Pad Oxide
- Deposit 1500A Si_3N_4 by LPCVD

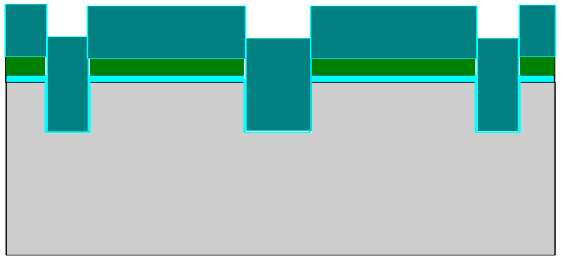
- Level 1 Lithography to protect Active areas with photoresist

- STI Trench Etch
- RIE in Drytek Quad
- Target: 4000A Si Trench

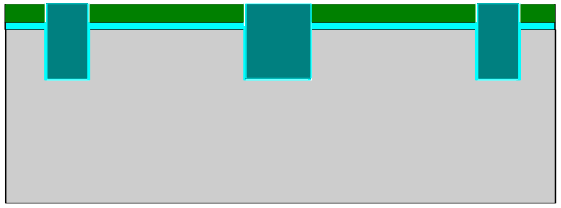
Example STI Process



- Remove photoresist
- Grow 500A Liner Oxide
- Repair damage to sidewalls

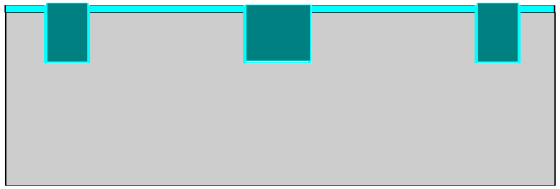


- Deposit 7000A TEOS SiO_2 by PECVD in Applied Materials P5000



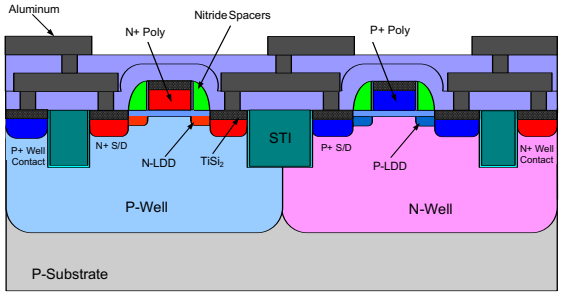
- CMP TEOS with Westech 372
- Nitride is stopping layer since CMP slurry removes oxide 4x faster then nitride

Example STI Process



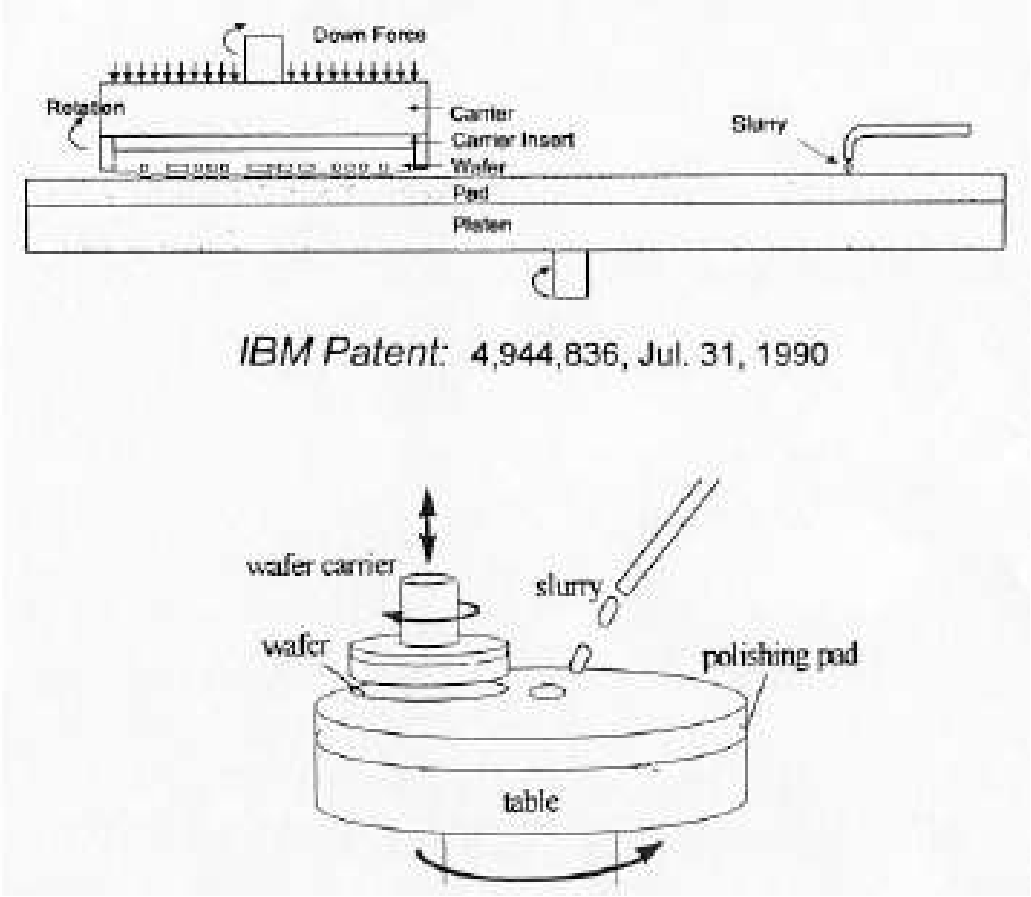
- Densify TEOS in Bruce Furnace for 60 min @ 1000C in N_2
- Remove Nitride in Phosphoric Acid (H_3PO_4) @ 175C

- Many more steps . . .



- Final CMOS Cross Section

CMP Equipment Schematic



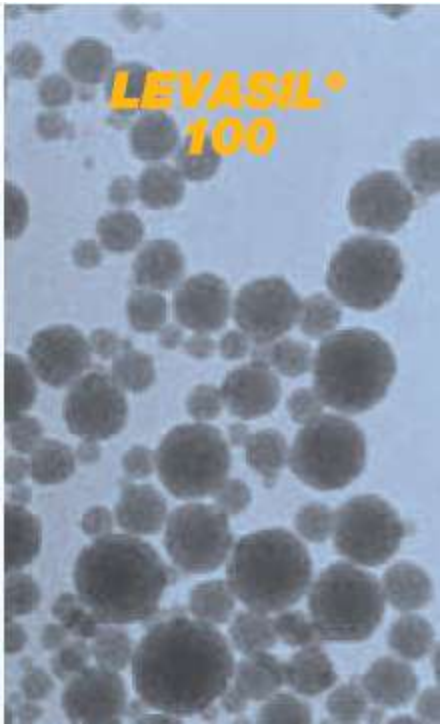
Speedfam/IPEC/Westech Model 372

Note: The carrier oscillates as well as the table to improve uniformity

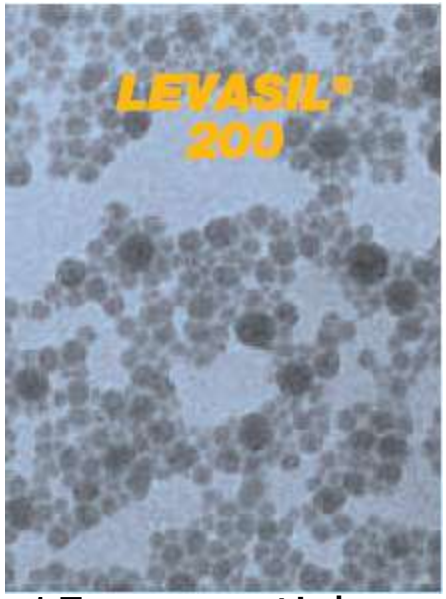
Pads and Slurry

- Current pad on Westech 372 is a Rodel CR IC1000-A2, 23” diameter
- Small circular pits for pattern. Others have rings, diamonds, checkerboard, etc
- Diamond grit pad conditioner will rough up surface of pad to increase friction with wafer and maintain etch rate and uniformity
- Slurries are colloidal silica particles of sub-micron size in KOH or NH_4OH with pH of 10.
- Claims by Rodel Corp. of Cerium dioxide (CeO_2) slurry with selectivity to nitride as high as 200:1

H.C. Stark LEVASIL Brand Slurries



30 nm particles



15 nm particles

9 nm particles

*LEVASIL 50 ->55 nm particles

- We have LEVASIL 50/20%, 100/45%, 200/30%, and 50/50% (on order)
- First number is specific area of particles in m^2/g (smaller means bigger)
- Second number is % solid in solution (larger means more particles)

http://www.hcstarck.de/pages/137/levasil_eng_2004_web9872.pdf

Westech 372 “How-to” & Process Knobs

- **Carrier Speed** (10-100 RPM, too fast and wafer can hydroplane across pad)
- **Table Speed** (10-100 RPM, for slurry distribution)
- **Down Force** (4 to 10 PSI, too low and wafer can hydroplane, too high and wafer can break)
- **Slurry Flow** (10 - 100 mL/min)

- The computer displays various outputs to monitor:
- **Pad Temp** (76-80 degrees F)
- **Carrier Current** (3-5 Amps)
- **Wafer Pressure** (# not correct, computer can’t control the down force automatically)

Wafer Pressure Calculation

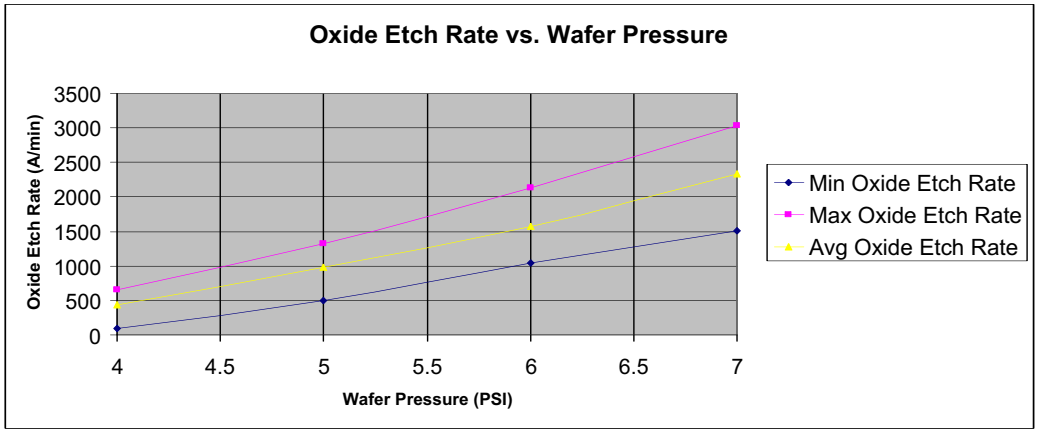
- Down Force/Wafer Pressure is controlled by gauge on side of tool. 80 PSI on gauge is 500 lbs of down force distributed over the area of 6” wafer (28.26 sq. in.)

- Wafer Pressure = 0.2211 * Gauge Pressure

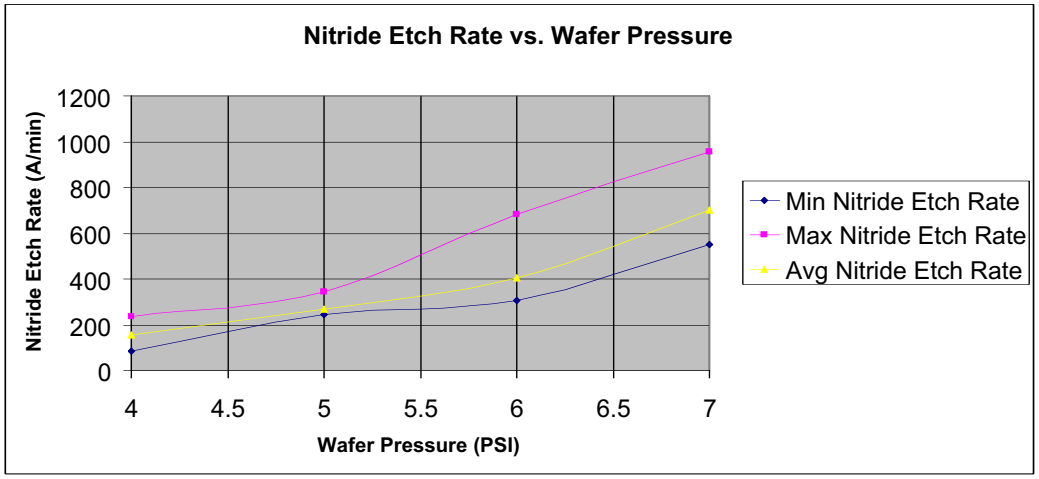
Gauge (PSI)	Wafer (PSI)
18	4
22	5
27	6
32	7

Note: The Westech will not engage the down force and timer will not begin unless gauge pressure is below 10 PSI.

CMP Characterization

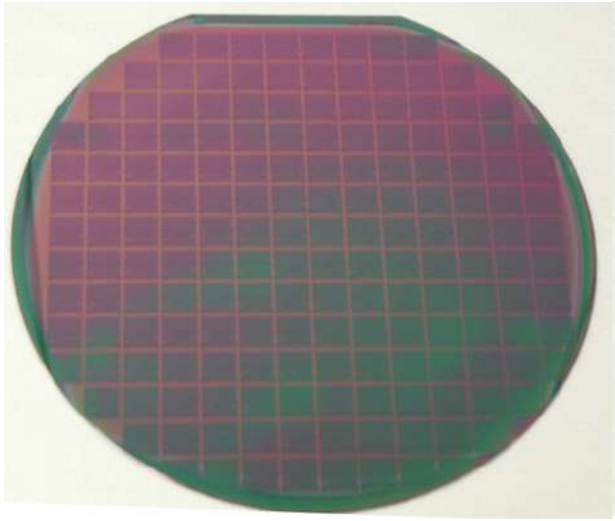


Wafer Pressure	Ox/Nit Selectivity	Non Uniformity (%)	
(PSI)	Avg	Oxide	Nitride
4	2.79	73.51	48.13
5	3.64	45.24	17.01
6	**3.87**	**34.32**	**38.13**
7	3.32	33.39	26.95

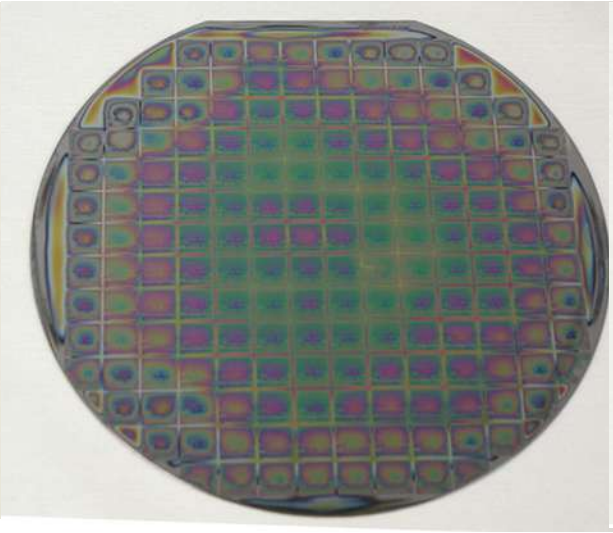


MIKESTI Process uses:
Carrier Speed = 70 RPM
Table Speed = 50 RPM
Wafer Pressure = **6 PSI**
Slurry Flow = 60 mL/min
Carrier Vacuum = Off

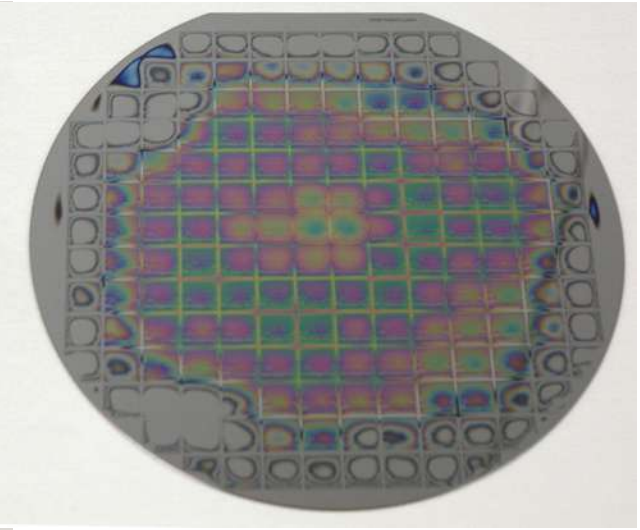
Results using MIKESTI Process



Wafer C10 before CMP



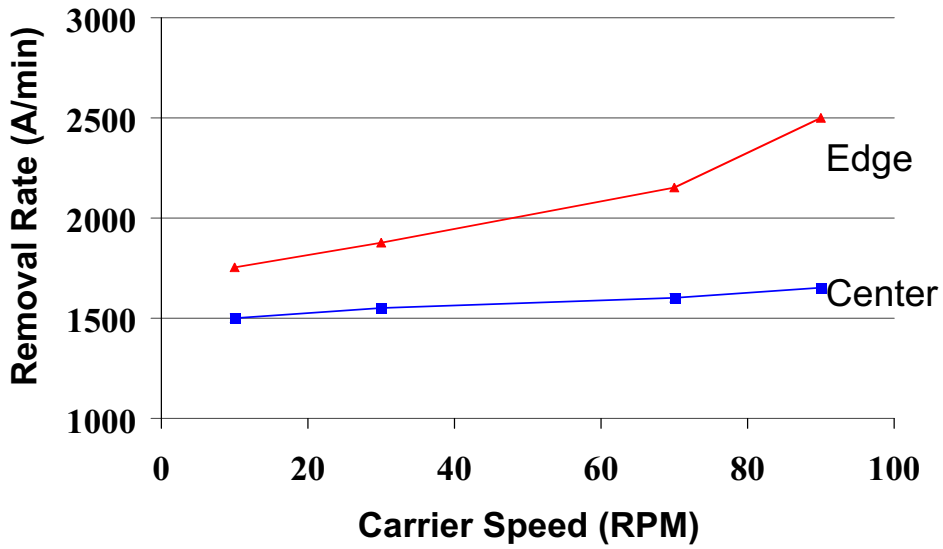
After 5 minutes of Polishing



After 9.5 minutes of Polishing

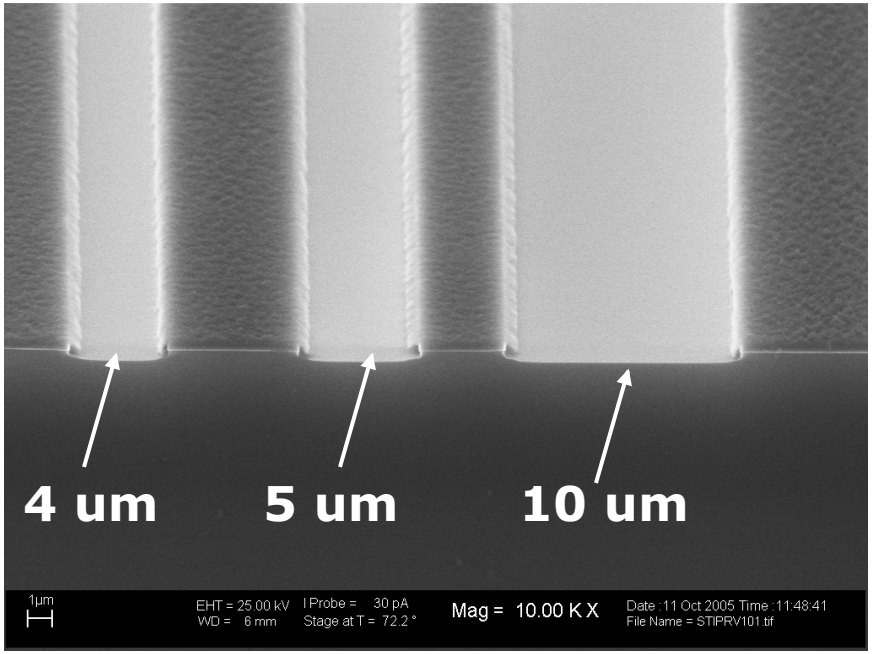
- Edges are polishing faster than center of wafer
- ~4” diameter of 6” wafer is useable

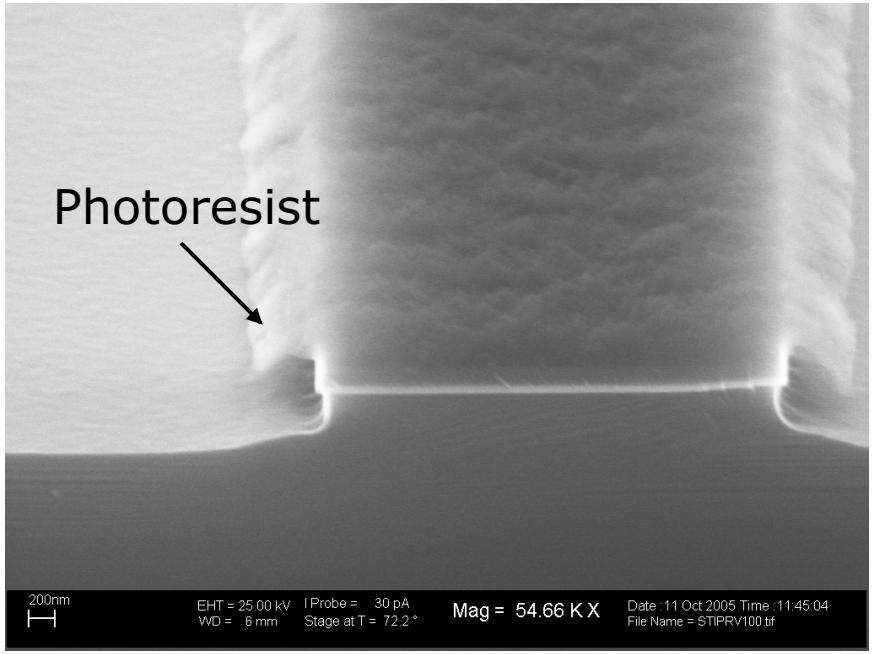
Edge vs. Center Removal Rate



- This plot is from Intel Corp. and illustrates the difference between center and edge removal for CMP
- Westech 472 and beyond has ability to apply back pressure to wafer (0-2 PSI is typical) to improve the center-edge non-uniformity

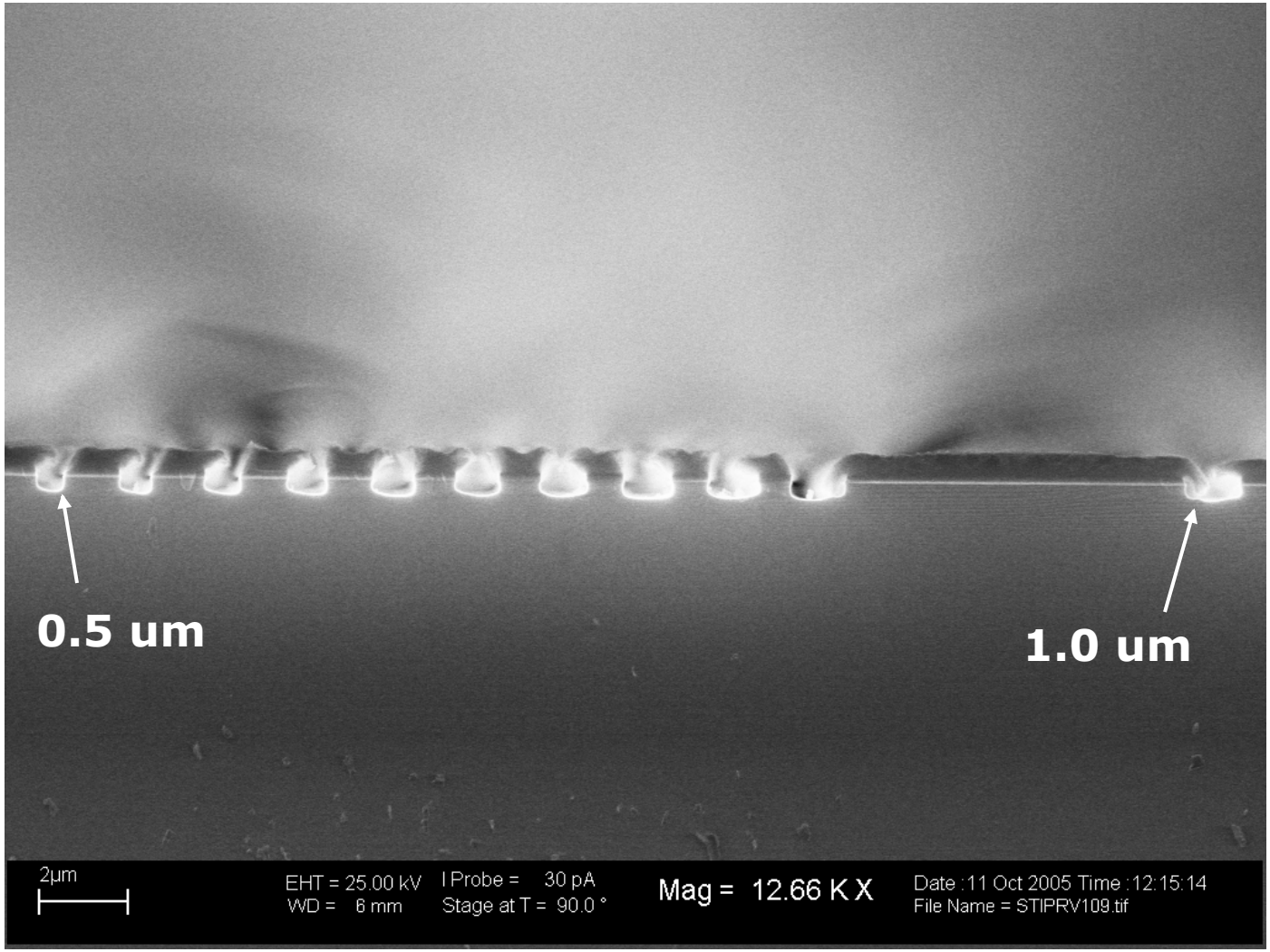
Anisotropic RIE of Silicon in Drytek Quad



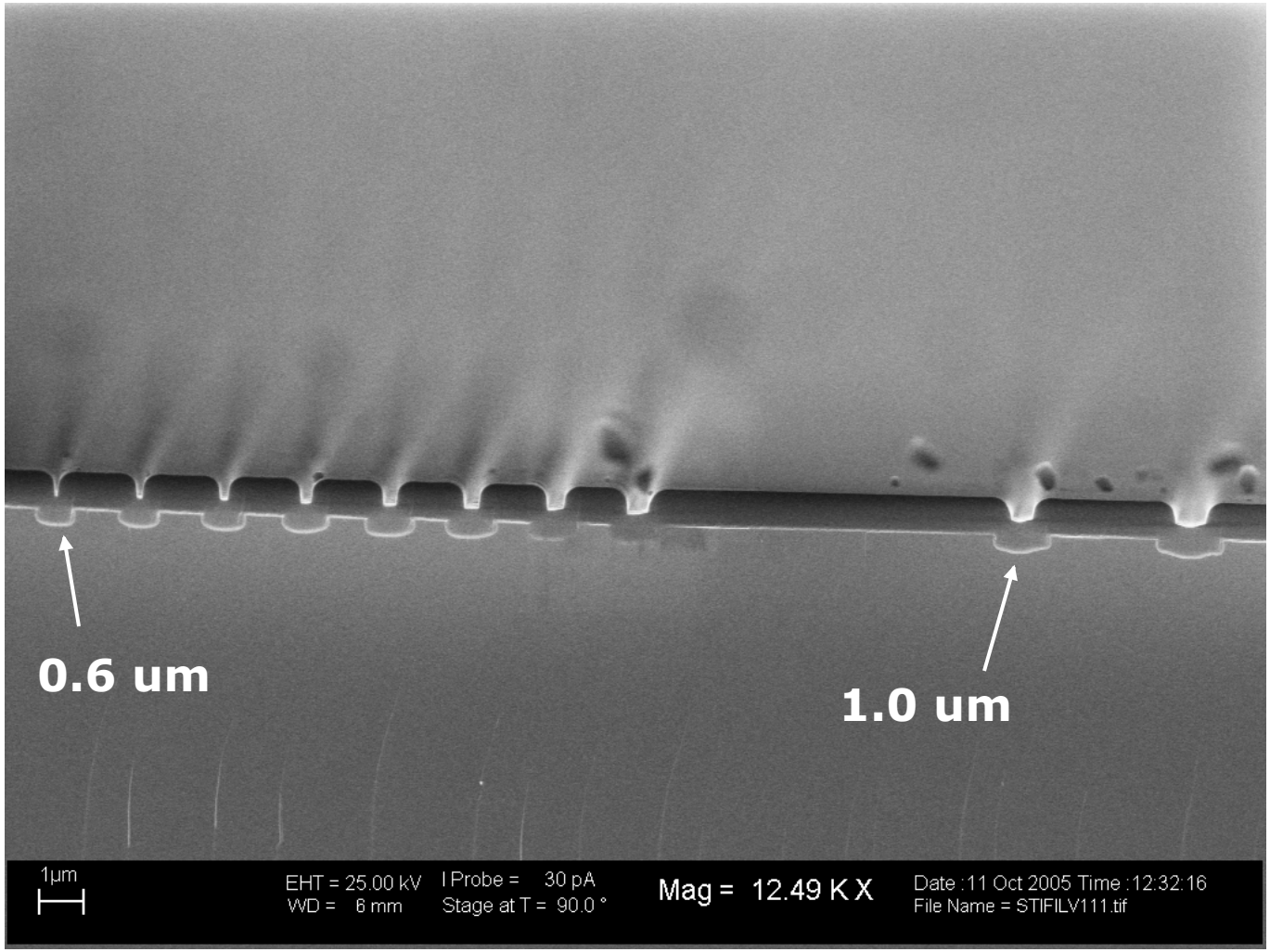


- Photoresist is flopping over at end of etch, masking the last minute of Si etch, as seen by the bump
- Need longer resist hard bake and maybe a lower power etch (less then 250W used for this recipe)
- Drytek Quad clearly is capable of anisotropic profiles

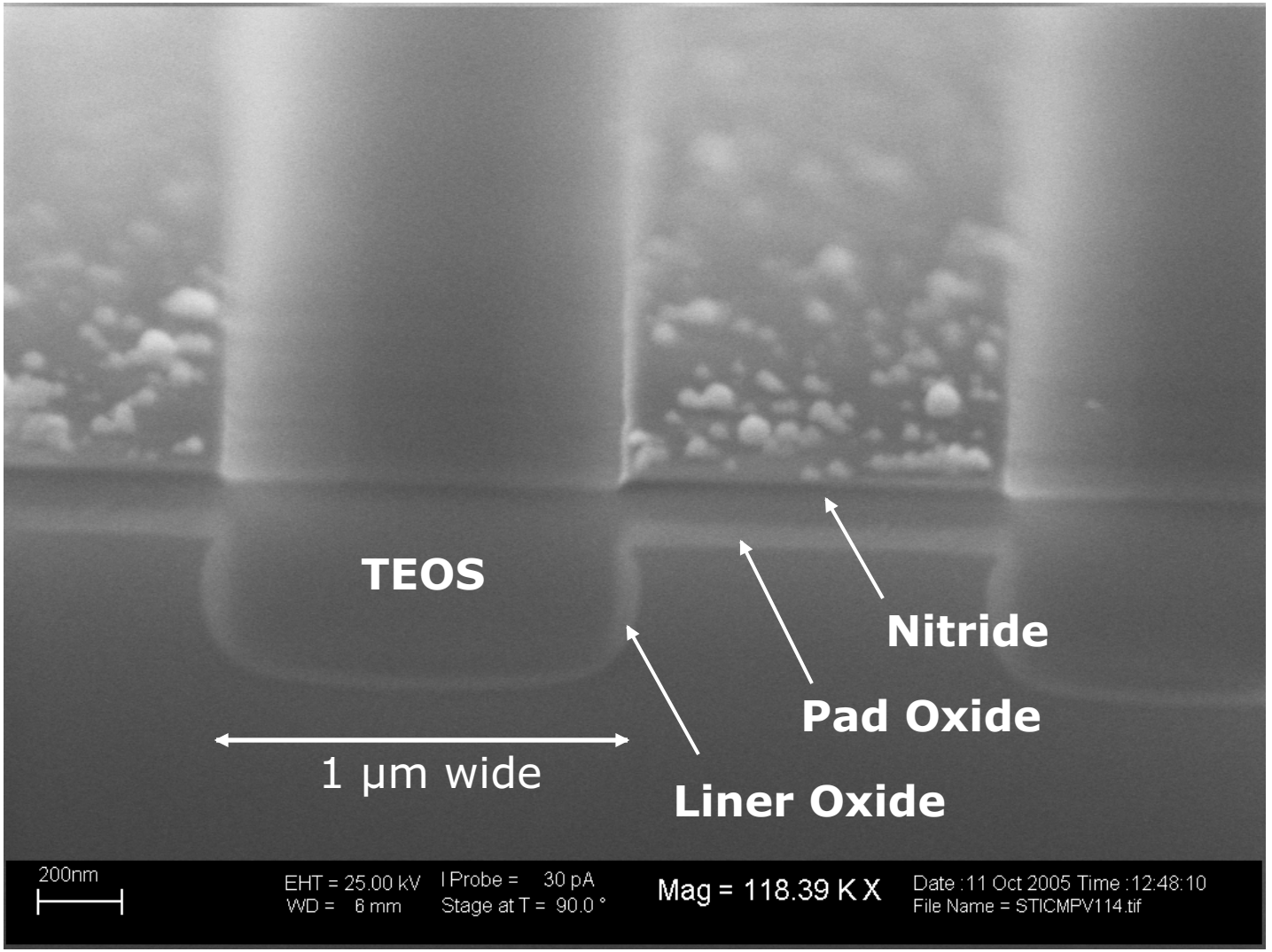
RIE Trench Etch with Photoresist



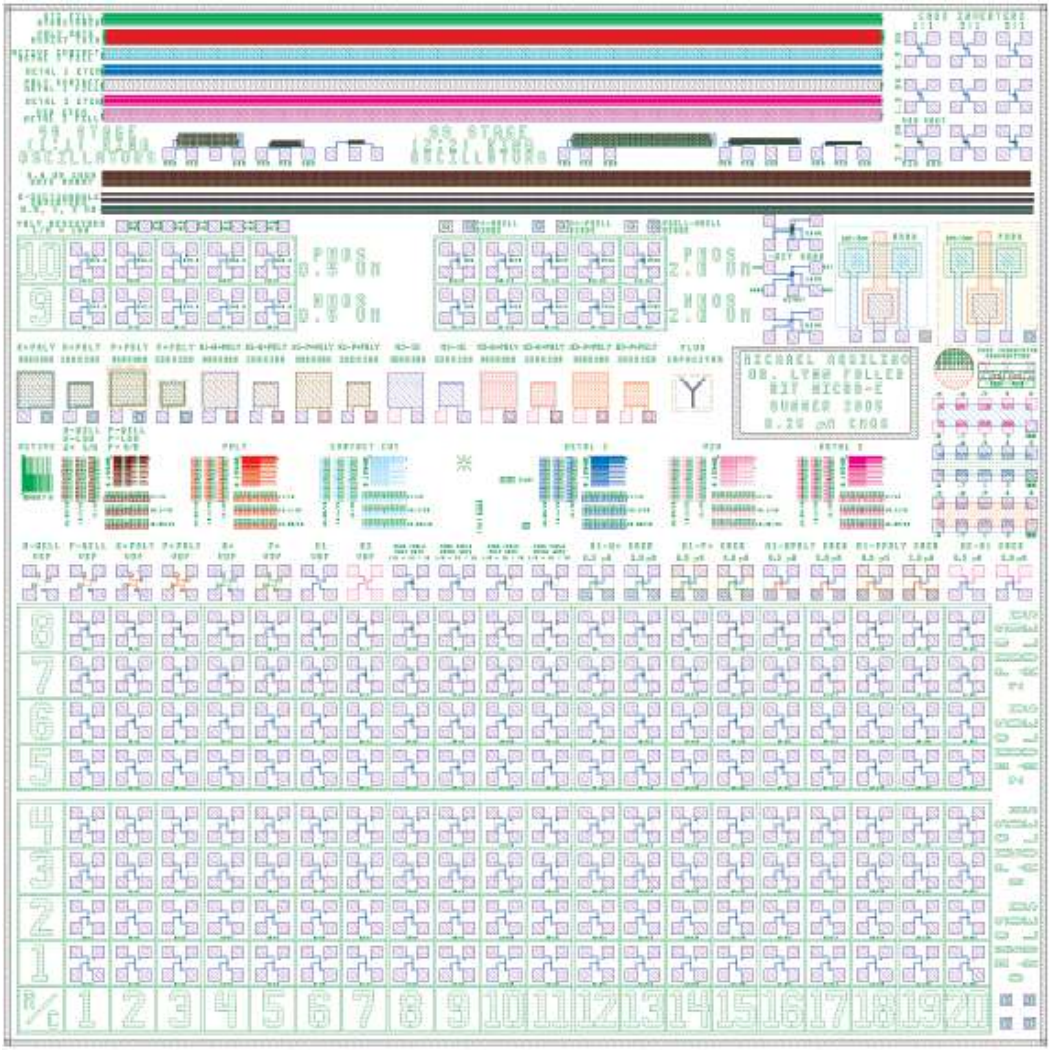
7000A Trench Fill with PECVD TEOS



SEM After CMP of Minimum Width Feature

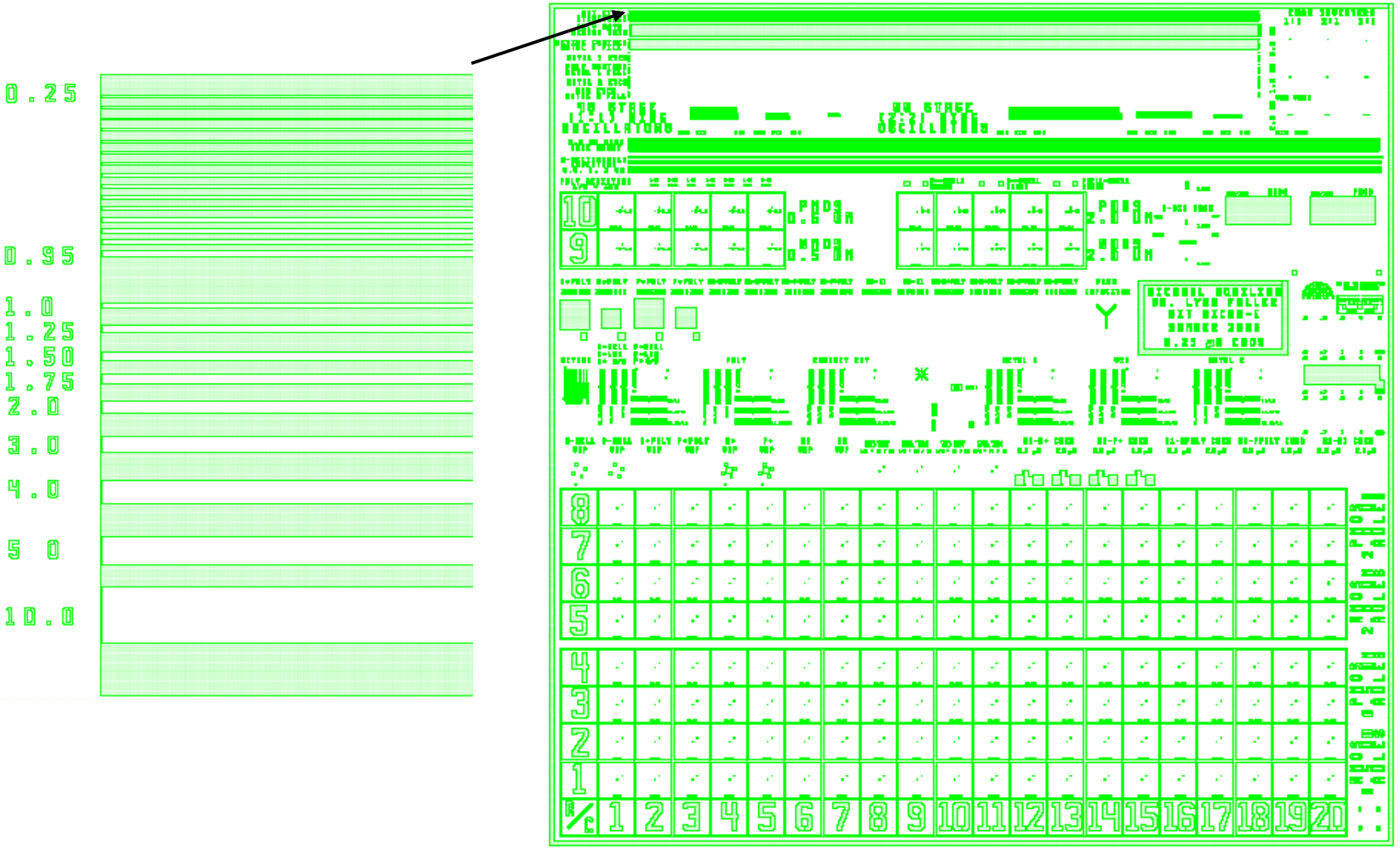


Test Chip Layout



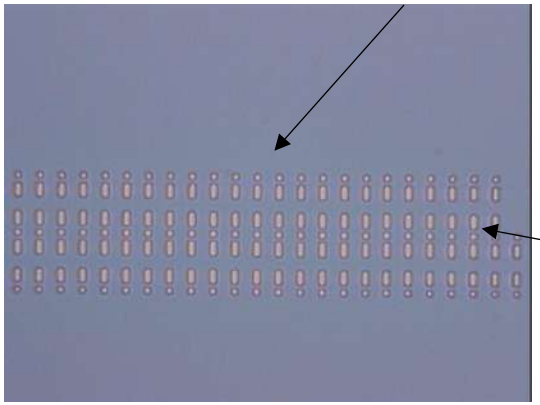
- 11 Design Layers
- 10 Masks
- 12 Lithography Levels

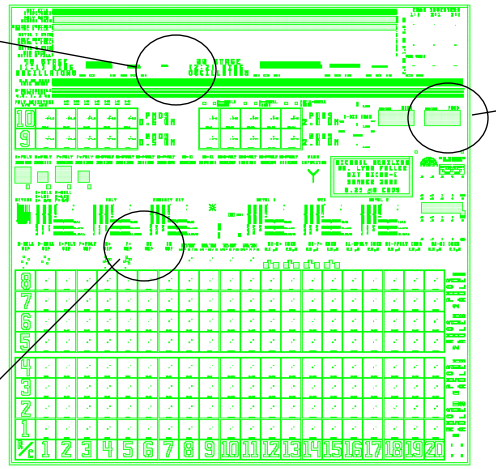
Active Layer of Test Chip only

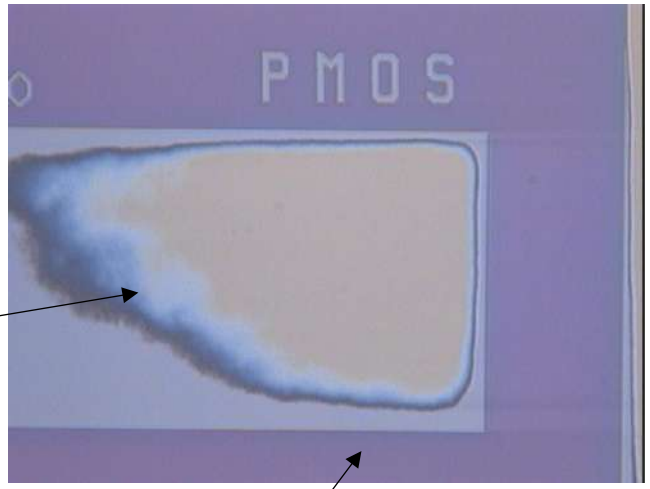


Area Dependence of CMP

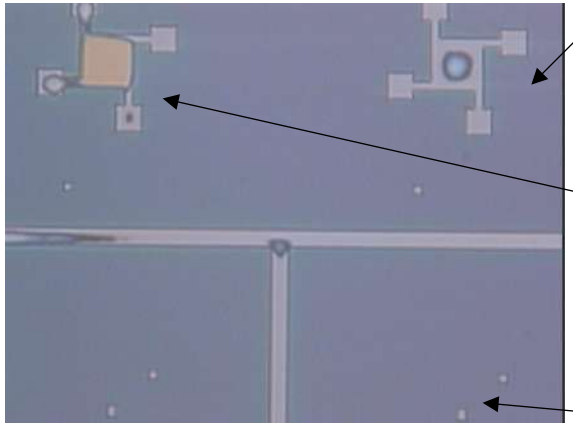
Nitride Clear over Small Active Areas







Nitride removal rate greatly reduced at edge of chip due to nitride streets



Some Nitride remains over larger areas

Nitride Clear over Small Active Areas

Process/Layout Challenges

- CMP is strongly dependent on pattern density
- Small areas polish faster
- Dense areas polish slower and reduce dishing of the field oxide

- Each layout will require a different polish time

- Dummy structures should be added to reduce the pattern density dependence

- Active mask should be redesigned to allow for clear field streets. This will prevent the edges of the chips from polishing slower since pad will not be supported by large active area streets

References

http://www.cnf.cornell.edu/doc/CMP%2520Primer.pdf

http://www.erc.arizona.edu/Education/MME%20Course%20Materials/MME%20Modules/CMP%20Module/CMP%20Tutorial.ppt

http://www.rit.edu/~lffeee/lec_cmp.pdf

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